Claims

What is claimed is:

1. A latch comprising:

a clocked trans-admittance stage circuit for receiving a voltage and producing a current output; and

an active load connected to receive as input the current output of said trans-admittance circuit and produce a voltage output.

2. The latch in accordance with claim 1, wherein the active load is a trans-impedance stage circuit.

3. The latch in accordance with claim 1, wherein said trans-admittance stage circuit comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

4. The latch in accordance with claim 3, wherein the base of said first and second ~~transmitters~~ transistors being clocked on opposite phases of a clock signal.

5. The latch in accordance with claim 4, wherein the base of said third transistor receives as input a voltage signal and the base of said fourth transistor receives as input an inverted voltage signal, said third transistor produces a current output signal based on the inverted voltage signal, and said fourth transistor produces an inverted current output signal based on the voltage signal.

6. The latch in accordance with claim 1, further comprising transmission lines coupled between said clocked trans-admittance circuit and said active load.

7. A cascaded latch chain comprising:

a clocked trans-admittance stage latch receiving an input voltage and producing an output current.

8. The cascaded latch in accordance with claim 7, further comprising at least one latch pair connected to receive the output current of said clocked trans-admittance stage latch and producing an output current, said at least one latch pair including two independent combined trans-admittance and trans-impedance stages.

9. The cascaded latch chain in accordance with claim 8, comprising at least two latch pairs including a first latch pair and a last latch pair, each latch pair having two independent trans-admittance and trans-impedance stages, the two trans-admittance and trans-impedance stages of each latch pair being clocked on opposite phases of a clock signal.

10. The cascaded latch chain in accordance with claim 9, wherein said trans-admittance stage in each latch pair comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter

of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

11. The cascaded latch chain in accordance with claim 9, wherein the two trans-admittance and trans-impedance stages in said at least one latch pair are clocked on opposite phases of a clock signal.

12. The cascaded latch chain in accordance with claim 7, further comprising a trans-impedance stage latch connected to receive the output current of the last latch pair and produce an output voltage.

13. The cascaded latch chain in accordance with claim 8, further comprising a trans-impedance stage latch connected to receive the output current of the last latch pair and produce an output voltage.

14. A latch pair comprising:

two independent combined trans-admittance and trans-impedance stages.

15. The latch pair in accordance with claim 14, wherein each trans-admittance stage comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter

of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

16. The latch pair in accordance with claim 14, wherein the two trans-admittance and trans-impedance stages are clocked on opposite phases of a clock signal.